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Kazuhisa Fujimoto

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MATTINGLY & MALUR, P.C.  
1800 DIAGONAL ROAD  
SUITE 370  
ALEXANDRIA, VA 22314

EXAMINER

SAVLA, ARPAN P

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/820,964	<b>Applicant(s)</b> FUJIMOTO ET AL.	
	<b>Examiner</b> Arpan P. Savla	<b>Art Unit</b> 2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 04 August 2009.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 21,23-25,27,29-39 and 44-55 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 21,23-25,27,29-39 and 44-55 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 April 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### **Continued Examination Under 37 CFR 1.114**

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 4, 2009 has been entered.

### **Response to Amendment**

This Office action is in response to Applicant's communication filed August 4, 2009 in response to the Office action dated April 7, 2009. Claims 21, 27, 31-39, and 53 have been amended. New claim 55 has been added. Claims 21, 23-25, 27, 29-39, and 44-55 are pending in this application.

### **Terminal Disclaimer**

1. The terminal disclaimer filed on August 4, 2009 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of any patent granted on Application Number 11/031,556 has been reviewed and is accepted. The terminal disclaimer has been recorded.

## **OBJECTIONS**

### **Drawings**

2. Figures 20 and 21 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

## **REJECTIONS NOT BASED ON PRIOR ART**

### **Double Patenting**

3. In view of the terminal disclaimer discussed above, the provisional obviousness-type double patenting rejection of **claims 21, 23-25, 27, 29-39, and 44-54** has been withdrawn.

### **Claim Rejections - 35 USC § 103**

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. **Claims 21-28 and 30-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis et al. (U.S. Patent 6,343,324) (hereinafter “Hubis”) in view of Klein (U.S. Patent 6,108,732) and Alford, Jr. (U.S. Patent Application Publication 2003/015884) (hereinafter “Alford”).**

3. **As per claim 21**, Hubis discloses a storage system comprising:

a plurality of disk drives configuring at least one logical volume (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter controlling to store data, which are sent from at least one host computer to said at least one logical volume (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180); *It should be noted that the “Processor 180” is equivalent to the “processor adapter”.*

a plurality of first interface adapters each coupled to said at least one host computer and receiving a write request and data sent from said at least one host computer and sending a first control information related to said write request to at least one of said processor adapters and sending data received at each of said first interface adapters based on a second control information sent from said at least one processor adapter (col. 7, line 64 – col. 8, line 5; col. 15, lines 19-25; col. 15, line 67 – col. 16, line 3; Fig. 2A, elements 184-1 - 184-M); *It should be noted that the “I/O Processors 184-1-M” are equivalent to the “plurality of first interface adapters”.*

a cache memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig.

2A, element 186); *It should be noted that the "Data Cache Memory" is equivalent to the "cache memory adapter".*

a plurality of second interface adapters each coupled to said disk drives and receiving data stored in said cache memory adapter asynchronously with receipt of said write request at said first interface adapters from said cache memory adapter based on a third control information sent from said at least one processor adapter and storing data received at each of said second interface adapters in said disk drives (col. 7, line 64 – col. 8, line 5; col. 15, line 67 – col. 16, line 6; Fig. 2A, elements 185-1 - 184-5); *It should be noted that the "I/O Processors 185-1-M" are equivalent to the "plurality of second interface adapters".*

a switch adapter coupled to said processor adapters, said first interface adapters, said cache memory adapter and said second interface adapters and relaying data between said first interface adapters and said cache memory adapter and relaying data between said cache memory adapter and said second interface adapters (col. 15, lines 63-66; Fig. 2A, element 183); *It should be noted that the "PCI Bus Interface and Memory Controller" is equivalent to the "switch adapter".*

wherein said processor adapter can access to each of said first interface adapters and each of said second interface adapters (col. 16, lines 6-9).

Hubis does not disclose a plurality of processor adapters;

wherein the number of said processor adapters are increased or decreased independently of the first and second interface adaptor, the memory adaptor and the switch adaptor, based on a required performance.

Klein discloses a plurality of processor adapters (col. 3, lines 23-29; Fig. 1, elements 102, 108, 114, and 120; col. 4, lines 33-34; Fig. 2, element 200); *It should be noted that the "processor modules" are equivalent to the "processor adapters"*.

wherein a number of said processor adapters is increased or decreased independently of the first and second interface adaptor, the memory adaptor and the switch adaptor, based on a required performance (col. 4, line 56 – col. 5, line 37; col. 5, line 49 – col. 6, line 12; Figs. 3 and 4);

wherein each of said processor adapters includes a plurality of processors (col. 3, lines 1-3).

Hubis and Klein are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Klein's adding or removing processor modules technique to Hubis' storage system. The motivation for doing so would have been to allow a processor module to be removed from a computer system and replaced without shutting the computer system down. This allows failed processor modules to be replaced and processor modules to be upgraded, while the computer system continues to operate, thus, greatly improving computer system reliability.

The combination of Hubis/Klein does not disclose when a first processing load at said first interface adapters which are coupled to said at least one host computer is greater than a second processing load at said second interface adapters which are coupled to said disk drives, the number of processors allocated to said first processing

load at said first interface adapters is larger than the number of processors allocated to said second processing load at said second interface adapters,

and wherein when said second processing load of said second interface adapters is greater than said first processing load at said first interface adapters, the number of processors allocated to said second processing load of said second interface adapters is larger than the number of said first processing load of said first interface adapters.

Alford discloses when a first processing load at said first interface adapters is greater than a second processing load at second interface adapters, the number of processors allocated to said first processing load at said first interface adapters is larger than the number of processors allocated to said second processing load at said second interface adapters (paragraphs 0043-0044 and 0048-0049; Fig. 4; Fig. 7), *It should be noted that the "processing capacity" in the "overloaded partition" is equivalent to the "first processing load" and said partition's "I/O slots" are equivalent to the "first interface adapters". It should also be noted that the "processing capacity" in the "partition that is either idle or is operating below a minimum threshold" is equivalent to the "second processing load" and said partition's "I/O slots" are equivalent to the "second interface adapters". Lastly, in the case that both partitions were allocated two CPUs each before the dynamic re-assignment process, after the re-assignment process the "overloaded partition" would be allocated three CPUs while the "partition that is either idle or is operating below a minimum threshold" would be allocated one CPU.*



and when said second processing load of said second interface adapters is greater than said first processing load at said first interface adapters, the number of processors allocated to said second processing load of said second interface adapters is larger than the number of said first processing load of said first interface adapters (paragraphs 0043-0044 and 0048-0049; Fig. 4; Fig. 7). *In this reverse case, it should be noted that the "processing capacity" in the "overloaded partition" is equivalent to the "second processing load" and said partition's "I/O slots" are equivalent to the "second interface adapters". It should also be noted that the "processing capacity" in the "partition that is either idle or is operating below a minimum threshold" is equivalent to the "first processing load" and said partition's "I/O slots" are equivalent to the "first interface adapters". Lastly, in the case that both partitions were allocated two CPUs each before the dynamic re-assignment process, after the re-assignment process the "overloaded partition" would be allocated three CPUs while the "partition that is either idle or is operating below a minimum threshold" would be allocated one CPU.*

The combination of Hubis/Klein and Alford are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Alford's dynamic re-assignment of resources within Hubis/Klein's storage system, such that one partition is coupled to the host computer and another partition is coupled to the disk drives. The motivation for doing so would have been to communicate information about peaks in resource demands from an

operating system running in a partition to the partitioning management software such that the software can re-assign additional resources to the partition as needed.

4. **As per claim 23**, the combination of Hubis/Klein/Alford discloses said processor adapters are assigned to a process of at least one of said first interface adapters and a process of at least one of said second interface adapters (Hubis, col. 16, lines 6-9).

5. **As per claim 24**, the combination of Hubis/Klein/Alford discloses said at least one processor adapter is assigned to said plurality of first interface adapters (Hubis, col. 16, lines 6-9).

6. **As per claim 25**, the combination of Hubis/Klein/Alford discloses said at least one processor adapter is assigned to said plurality of second interface adapters (Hubis, col. 16, lines 6-9).

7. **As per claim 27**, the combination of Hubis/Klein/Alford discloses it is possible to change the number of said processor adapters upon storing data in said disk drives (Klein, col. 4, line 56 – col. 5, line 37; col. 5, line 49 – col. 6, line 12; Figs. 3 and 4).

8. **As per claim 30**, the combination of Hubis/Klein/Alford discloses said first control information is used to notify said at least one processor adapter of receiving said write request (Hubis, col. 15, lines 10-25).

9. **As per claim 31**, the combination of Hubis/Klein/Alford discloses said at least one processor adapter detects an area of said memory in which data of said at least one logical volume need to be stored in accordance with said received first control information (Hubis, col. 15, lines 19-25; col. 16, line 67 – col. 17, line 9). *It should be noted that it is inherently required Processor 180 detect/recognize an area of the Data*

*Cache Memory in order to allocate space for storing data in the Cache Memory during a write task.*

10. **As per claim 32**, the combination of Hubis/Klein/Alford discloses said second control information includes information related to an area of said memory in which data received at each of said first interface adapters need to be stored (Hubis, col. 15, lines 19-25; col. 16, line 67 – col. 17, line 9). *It should be noted that it is inherently required Processor 180 allocate/reserve an area of the Data Cache Memory in order to store data in the Cache Memory during a write task.*

11. **As per claim 33**, the combination of Hubis/Klein/Alford discloses said at least one processor adapter finds an area of said disk drives related to said at least one logical volume for storing data of said at least one logical volume based on said received first control information (Hubis, col. 15, lines 23-25; col. 16, lines 6-9).

12. **As per claim 34**, the combination of Hubis/Klein/Alford discloses said third control information includes information related to an area of said disk drives in which data received at each of said second interface adapters need to be stored (Hubis, col. 15, lines 23-25; col. 16, lines 6-9).

13. **As per claim 35**, the combination of Hubis/Klein/Alford discloses said at least one processor adapter controls to create a parity data of RAID (Redundant Array of Inexpensive Disks) from data received by at least one of said first interface adapters (Hubis, col. 4, line 64 – col. 5, line 3).

14. **As per claim 36**, Hubis discloses a storage system coupled a host computer, said storage system comprising:

at least one disk drive configuring at least one logical volume (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter controlling to store data by determining a location at which the data should be stored, the data being sent from said host computer to said at least one logical volume for updating said logical volume, in said at least one disk drive (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a first interface adapter coupled to said host computer and receiving a write request and data sent from said host computer and sending a first control information related to said write request to said processor adapter and sending data received at said first interface adapter based on a second control information sent from said processor adapter (col. 7, line 64 – col. 8, line 5; col. 15, lines 19-25; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1); *It should be noted that the “I/O Processor 184-1” is equivalent to the “first interface adapter”.*

a cache memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

a second interface adapter coupled to said at least one disk drive receiving data stored in said cache memory adapter from said cache memory adapter based on a third control information sent from said processor adapter asynchronously with the receipt of said write request at said first interface adaptor and storing data received at said second interface adapter in said at least one disk drive (col. 7, line 64 – col. 8, line 5; col. 15,

line 67 – col. 16, line 6; Fig. 2A, element 185-1); *It should be noted that the “I/O Processor 185-1” is equivalent to the “second interface adapter”.*

a switch adapter coupled to said processor adapter, said first interface adapter, said cache memory adapter and said second interface adapter and relaying said data among said first interface adapter, said cache memory adapter and said second interface adapter (col. 15, lines 63-66; Fig. 2A, element 183);

Hubis does not disclose a plurality of processor adapters;

wherein the number of said processor adaptors are increased or decreased based on a required performance, even though the number of said first interface adapter, said cache memory adapter and said second interface adapter are not increased or decreased.

Klein discloses a plurality of processor adapters (col. 3, lines 23-29; Fig. 1, elements 102, 108, 114, and 120; col. 4, lines 33-34; Fig. 2, element 200);

wherein a number of said processor adaptors is increased or decreased based on a required performance, even though the number of said first interface adapter, said cache memory adapter and said second interface adapter are not increased or decreased (col. 4, line 56 – col. 5, line 37; col. 5, line 49 – col. 6, line 12; Figs. 3 and 4);

wherein each of said processor adapters includes a plurality of processors (col. 3, lines 1-3).

Hubis and Klein are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Klein's adding or removing processor modules technique to Hubis' storage system. The motivation for doing so would have been to allow a processor module to be removed from a computer system and replaced without shutting the computer system down. This allows failed processor modules to be replaced and processor modules to be upgraded, while the computer system continues to operate, thus, greatly improving computer system reliability.

The combination of Hubis/Klein does not disclose when a first processing load at said first interface adapter which are coupled to said at least one host computer is greater than a second processing load at said second interface adapter which are coupled to said at least one disk drive, the number of processors allocated to said first processing load at said first interface adapter is larger than the number of processors allocated to said second processing load at said second interface adapter,

and wherein when said second processing load of said second interface adapter is greater than said first processing load at said first interface adapter, the number of processors allocated to said second processing load of said second interface adapter is larger than the number of said first processing load of said first interface adapter.

Alford discloses when a first processing load at said first interface adapter is greater than a second processing load at second interface adapter, the number of processors allocated to said first processing load at said first interface adapter is larger than the number of processors allocated to said second processing load at said second interface adapter (paragraphs 0043-0044 and 0048-0049; Fig. 4; Fig. 7),

and when said second processing load of said second interface adapter is greater than said first processing load at said first interface adapter, the number of processors allocated to said second processing load of said second interface adapter is larger than the number of said first processing load of said first interface adapter (paragraphs 0043-0044 and 0048-0049; Fig. 4; Fig. 7).

The combination of Hubis/Klein and Alford are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Alford's dynamic re-assignment of resources within Hubis/Klein's storage system, such that one partition is coupled to the host computer and another partition is coupled to the disk drive. The motivation for doing so would have been to communicate information about peaks in resource demands from an operating system running in a partition to the partitioning management software such that the software can re-assign additional resources to the partition as needed.

15. **As per claim 37**, Hubis discloses a storage system coupled a host computer, said storage system comprising:

at least one disk drive configuring at least one logical volume (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter controlling to store data by determining a location at which the data should be stored, the data being sent from said host computer to said at least one logical volume for updating said at least one logical volume, in said at least one disk drive (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a first interface adapter coupled to said host computer and receiving data sent from said host computer and sending data received at said first interface adapter based on a first control information sent from said processor adapter (col. 7, line 64 – col. 8, line 5; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1);

a cache memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

a second interface adapter coupled to said at least one disk drive receiving data stored in said cache memory adapter from said cache memory adapter based on a second control information sent from said processor adapter asynchronously with receipt of said data at said first interface adapter and storing said data received at said second interface adapter in said at least one disk drive (col. 7, line 64 – col. 8, line 5; col. 15, line 67 – col. 16, line 6; Fig. 2A, element 185-1);

a switch adapter coupled to said processor adapter, said first interface adapter, said cache memory adapter and said second interface adapter and relaying data of said at least one logical volume among said first interface adapter, said cache memory adapter and said second interface adapter and not relaying data of said at least one logical volume to said processor adapter (col. 15, lines 63-66; Fig. 2A, element 183); *It should be noted that when the host sends a read request to the logical volumes, Processor 180 does not receive the read data itself, but rather controls the process of sending the read data back to the host.*



wherein it is possible to change the number of said processor adapters, independently of the first and second interface adapters, the memory adaptor and the switch adaptor, upon storing on storing data in said disk drive and based on a required performance.

Klein discloses a plurality of processor adapters (col. 3, lines 23-29; Fig. 1, elements 102, 108, 114, and 120; col. 4, lines 33-34; Fig. 2, element 200);

wherein it is possible to change the number of said processor adapters, independently of the first and second interface adapters, the memory adaptor and the switch adaptor, upon storing on storing data in said at least one disk drive and based on a required performance (col. 4, line 56 – col. 5, line 37; col. 5, line 49 – col. 6, line 12; Figs. 3 and 4);

wherein each of said processor adapters includes a plurality of processors (col. 3, lines 1-3).

Hubis and Klein are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Klein's adding or removing processor modules technique to Hubis' storage system. The motivation for doing so would have been to allow a processor module to be removed from a computer system and replaced without shutting the computer system down. This allows failed processor modules to be replaced and processor modules to be upgraded, while the computer system continues to operate, thus, greatly improving computer system reliability.

The combination of Hubis/Klein does not disclose when a first processing load at said first interface adapter which are coupled to said at least one host computer is greater than a second processing load at said second interface adapter which are coupled to said at least one disk drive, the number of processors allocated to said first processing load at said first interface adapter is larger than the number of processors allocated to said second processing load at said second interface adapter,

and wherein when said second processing load of said second interface adapter is greater than said first processing load at said first interface adapter, the number of processors allocated to said second processing load of said second interface adapter is larger than the number of said first processing load of said first interface adapter.

Alford discloses when a first processing load at said first interface adapter is greater than a second processing load at second interface adapter, the number of processors allocated to said first processing load at said first interface adapter is larger than the number of processors allocated to said second processing load at said second interface adapter (paragraphs 0043-0044 and 0048-0049; Fig. 4; Fig. 7),

and when said second processing load of said second interface adapter is greater than said first processing load at said first interface adapter, the number of processors allocated to said second processing load of said second interface adapter is larger than the number of said first processing load of said first interface adapter (paragraphs 0043-0044 and 0048-0049; Fig. 4; Fig. 7).

The combination of Hubis/Klein and Alford are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Alford's dynamic re-assignment of resources within Hubis/Klein's storage system, such that one partition is coupled to the host computer and another partition is coupled to the disk drive. The motivation for doing so would have been to communicate information about peaks in resource demands from an operating system running in a partition to the partitioning management software such that the software can re-assign additional resources to the partition as needed.

16. **As per claim 38**, Hubis discloses a storage system coupled a host computer, said storage system comprising:

a at least one disk drive configuring at least one logical volume (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter which controls to store data by determining a location at which the data should be stored, the data being sent from said host computer to said at least one logical volume for updating said at least one logical volume, in said at least one disk drive (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a first interface adapter coupled to said host computer and receiving the data sent from the host computer (col. 7, line 64 – col. 8, line 5; col. 15, lines 19-25; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1);

a cache memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

a second interface adapter coupled to said at least one disk drive, said first interface adapter, said processor adapter, and said cache memory adapter (col. 16, lines 3-6; Fig. 2A, element 185-1);

a switch adapter coupled to said processor adapter, said first interface adapter, said cache memory adapter and said second interface adapter (col. 15, lines 63-66; Fig. 2A, element 183);

wherein said switch adapter relays data between said first interface adapter and said second interface adapter via said cache memory adapter among said first interface adapter, said processor adapter, said cache memory adapter and said second interface adapter based on control information transferred among said first interface adapter, said processor adapter and said second interface adapter of said first interface adapter, said processor adapter, said cache memory adapter, and said second interface adapter, the relaying of the data between said first interface adapter and said second interface adapter being done asynchronously with the receipt of the data by the first interface adapter from said host computer (col. 7, line 64 – col. 8, line 5; col. 15, lines 63-66; col. 15, line 67 – col. 16, line; Fig. 2A, elements 183 and 186). *It should be noted that Data Cache Memory buffers any data sent between I/O Processor 184-1 and I/O Processor 185-1.*

Hubis does not disclose a plurality of processor adapters;

wherein the number of said processor adapters are increased or decreased independently of the first and second interface adaptor, the memory adaptor and the switch adaptor, based on a required performance.

Klein discloses a plurality of processor adapters (col. 3, lines 23-29; Fig. 1, elements 102, 108, 114, and 120; col. 4, lines 33-34; Fig. 2, element 200);

wherein a number of said processor adapters is increased or decreased independently of the first and second interface adaptor, the memory adaptor and the switch adaptor, based on a required performance (col. 4, line 56 – col. 5, line 37; col. 5, line 49 – col. 6, line 12; Figs. 3 and 4);

wherein each of said processor adapters includes a plurality of processors (col. 3, lines 1-3).

Hubis and Klein are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Klein's adding or removing processor modules technique to Hubis' storage system. The motivation for doing so would have been to allow a processor module to be removed from a computer system and replaced without shutting the computer system down. This allows failed processor modules to be replaced and processor modules to be upgraded, while the computer system continues to operate, thus, greatly improving computer system reliability.

The combination of Hubis/Klein does not disclose when a first processing load at said first interface adapter which are coupled to said at least one host computer is greater than a second processing load at said second interface adapter which are coupled to said at least one disk drive, the number of processors allocated to said first

processing load at said first interface adapter is larger than the number of processors allocated to said second processing load at said second interface adapter,

and wherein when said second processing load of said second interface adapter is greater than said first processing load at said first interface adapter, the number of processors allocated to said second processing load of said second interface adapter is larger than the number of said first processing load of said first interface adapter.

Alford discloses when a first processing load at said first interface adapter is greater than a second processing load at second interface adapter, the number of processors allocated to said first processing load at said first interface adapter is larger than the number of processors allocated to said second processing load at said second interface adapter (paragraphs 0043-0044 and 0048-0049; Fig. 4; Fig. 7),

and when said second processing load of said second interface adapter is greater than said first processing load at said first interface adapter, the number of processors allocated to said second processing load of said second interface adapter is larger than the number of said first processing load of said first interface adapter (paragraphs 0043-0044 and 0048-0049; Fig. 4; Fig. 7).

The combination of Hubis/Klein and Alford are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Alford's dynamic re-assignment of resources within Hubis/Klein's storage system, such that one partition is coupled to the host computer and another partition is coupled to the disk drive. The motivation for doing so would

have been to communicate information about peaks in resource demands from an operating system running in a partition to the partitioning management software such that the software can re-assign additional resources to the partition as needed.

17. **As per claim 39**, Hubis discloses a storage system coupled a host computer, said storage system comprising:

at least one disk drive configuring at least one logical volume (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter controlling to store data by determining a location at which the data should be stored, the data being sent from said host computer to said at least one logical volume for updating said at least one logical volume, in said at least one disk drive (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a first interface adapter coupled to said host computer and receiving a write request and data sent from said host computer and sending a first control information related to said write request to said processor adapter and sending data received at said first interface adapter based on a second control information sent from said processor adapter (col. 7, line 64 – col. 8, line 5; col. 15, lines 19-25; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1);

a cache memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

a second interface adapter coupled to said at least one disk drive and receiving data stored in said cache memory adapter from said cache memory adapter based on a

third control information sent from said processor adapter asynchronously with receipt of said write request at said first interface adapter and storing data received at said second interface adapter in said at least one disk drive (col. 7, line 64 – col. 8, line 5; col. 15, line 67 – col. 16, line 6; Fig. 2A, element 185-1);

wherein said processor adapter is coupled to said first interface adapter and said second interface adapter and sends said second control information to said first interface adapter and sends said third control information to said second interface adapter (col. 16, lines 6-9);

wherein said first interface adapter sends data to said cache memory adapter among said processor adapter, said cache memory adapter and said second interface adapter (col. 15, line 67 – col. 16, line 3);

wherein said second interface adapter receives data from said cache memory adapter among said processor adapter, said cache memory adapter and said first interface adapter (col. 16, lines 3-6);

wherein said cache memory adapter receives data from said first interface adapter and said second interface adapter among said processor adapter, said first interface adapter and said second interface adapter (col. 15, line 67 – col. 16, line 6);

Hubis does not disclose a plurality of processor adapters;

wherein the number of said processor adapters are increased or decreased independently of the first and second interface adaptor and the memory adaptor, based on a required performance.



Klein discloses a plurality of processor adapters (col. 3, lines 23-29; Fig. 1, elements 102, 108, 114, and 120; col. 4, lines 33-34; Fig. 2, element 200);

wherein a number of said processor adapters is increased or decreased independently of the first and second interface adaptor and the memory adaptor, based on a required performance (col. 4, line 56 – col. 5, line 37; col. 5, line 49 – col. 6, line 12; Figs. 3 and 4);

wherein each of said processor adapters includes a plurality of processors (col. 3, lines 1-3).

Hubis and Klein are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Klein's adding or removing processor modules technique to Hubis' storage system. The motivation for doing so would have been to allow a processor module to be removed from a computer system and replaced without shutting the computer system down. This allows failed processor modules to be replaced and processor modules to be upgraded, while the computer system continues to operate, thus, greatly improving computer system reliability.

The combination of Hubis/Klein does not disclose when a first processing load at said first interface adapter which are coupled to said at least one host computer is greater than a second processing load at said second interface adapter which are coupled to said at least one disk drive, the number of processors allocated to said first

processing load at said first interface adapter is larger than the number of processors allocated to said second processing load at said second interface adapter,

and wherein when said second processing load of said second interface adapter is greater than said first processing load at said first interface adapter, the number of processors allocated to said second processing load of said second interface adapter is larger than the number of said first processing load of said first interface adapter.

Alford discloses when a first processing load at said first interface adapter is greater than a second processing load at second interface adapter, the number of processors allocated to said first processing load at said first interface adapter is larger than the number of processors allocated to said second processing load at said second interface adapter (paragraphs 0043-0044 and 0048-0049; Fig. 4; Fig. 7),

and when said second processing load of said second interface adapter is greater than said first processing load at said first interface adapter, the number of processors allocated to said second processing load of said second interface adapter is larger than the number of said first processing load of said first interface adapter (paragraphs 0043-0044 and 0048-0049; Fig. 4; Fig. 7).

The combination of Hubis/Klein and Alford are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Alford's dynamic re-assignment of resources within Hubis/Klein's storage system, such that one partition is coupled to the host computer and another partition is coupled to the disk drive. The motivation for doing so would

have been to communicate information about peaks in resource demands from an operating system running in a partition to the partitioning management software such that the software can re-assign additional resources to the partition as needed.

18. **As per claims 44-52**, the combination of Hubis/Klein/Alford discloses the cache memory adapter includes a control information memory module in which information for controlling data transfer is stored (Hubis, col. 15, line 67 – col. 16, line 3; col. 8, lines 2-5; Fig. 2A, element 186).

19. **As per claim 55**, the combination of Hubis/Klein/Alford discloses a plurality of said first interface adapters each receives a read request from at least one host computer (col. 8, lines 2-5; col. 15, line 67 – col. 16, line 2), and sends said read request to at least one of said processor adapters (col. 16, lines 6-9), and receives data corresponding to said read request from said cache memory based on a fourth control information sent from said at least one processor adapter (col. 15, lines 63-65).

20. **Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis in view of Klein and Alford as applied to claim 21 above, and further in view of Kuchta et al. (U.S. Patent 6,014,319) (hereinafter “Kuchta”).**

21. **As per claim 29**, the combination of Hubis/Klein does not disclose a first portion of said processor adapters are assigned to a process of at least one of said first interface adapters;

a second portion of said processor adapters are assigned to a process of at least one of said second interface adapters;

a proportion between said first portion and said second portion is decided in accordance with a proportion between a performance of said at least one first interface adapter and a performance of said at least one second interface adapter.

Kutcha discloses a first portion of said processor adapters are assigned to a process of at least one of said first interface adapters (col. 7, lines 15-18; Fig. 2A, element 245; Fig. 2B, elements 211-212); *It should be noted that "I/O modules 211-212" are equivalent to the "first portion of processor adapters" and "I/O cards 245" are equivalent to "first interface adapters"*.

a second portion of said processor adapters are assigned to a process of at least one of said second interface adapters (col. 7, lines 35-38; Fig. 2A, element 246; Fig. 2B, elements 209-210); *It should be noted that "I/O modules 209-210" are equivalent to the "second portion of processor adapters" and "I/O cards 246" are equivalent to "second interface adapters"*.

a proportion between said first portion and said second portion is decided in accordance with a proportion between a performance of said at least one first interface adapter and a performance of said at least one second interface adapter (col. 5, lines 59-63). *It should be noted that amount of I/O modules 209-210 versus the amount of I/O modules 211-212 (i.e. a proportion between said first portion and said second portion) is based on performance characteristics.*

The combination of Hubis/Klein and Kuchta are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Kuchta's additional I/O modules within Hubis/Klein's storage system. The motivation for doing so would have been to provide later system enhancements (Kuchta, col. 5, lines 49-50).

**22. Claims 53 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis in view of Klein, Alford, and Matsunami et al. (U.S. Patent Application Publication 2002/0091898) (hereinafter "Matsunami").**

**23. As per claim 53,** Hubis discloses a storage system comprising:

a plurality of disk drives (col. 7, lines 27-28; Fig. 2, element 108);

a plurality of first interface units each coupled to said at least one host computer and receiving a write request and data sent from said at least one host computer (col. 7, line 64 – col. 8, line 5; col. 15, lines 19-25; col. 15, line 67 – col. 16, line 3; Fig. 2A, elements 184-1 - 184-M);

a plurality of second interface units each coupled to said plurality of disk drives and storing the data in said plurality of disk drives asynchronously with the receipt of the write request at the first interface units (col. 7, line 64 – col. 8, line 5; col. 15, line 67 – col. 16, line 6; Fig. 2A, elements 185-1 - 185-M);

a processor unit separated from said first interface units and said second interface units (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a memory unit having at least one memory, said memory temporarily storing data sent from said first interface units (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

a switch unit coupled to said first interface units, said second interface units and said processor unit (col. 15, lines 63-66; Fig. 2A, element 183).

Hubis does not disclose a storage system comprising a first cluster system and a second cluster system,

a plurality of processor units;

wherein the switch unit of the first cluster system is coupled to the switch of the second cluster system by a communication path;

wherein the number of said processor units of the first cluster system and said second cluster system can be increased or decreased, independently of the first and second interface units, the memory units and the switch unit, based on a required performance.

Klein discloses a plurality of processor units (col. 3, lines 23-29; Fig. 1, elements 102, 108, 114, and 120; col. 4, lines 33-34; Fig. 2, element 200);

wherein the number of said processor units of the first cluster system and said second cluster system can be increased or decreased, independently of the first and second interface units, the memory units and the switch unit, based on a required performance (col. 4, line 56 – col. 5, line 37; col. 5, line 49 – col. 6, line 12; Figs. 3 and 4);

wherein each of said processor adapters includes a plurality of processors (col. 3, lines 1-3).

Hubis and Klein are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Klein's adding or removing processor modules technique to Hubis' storage system. The motivation for doing so would have been to allow a processor module to be removed from a computer system and replaced without shutting the computer system down. This allows failed processor modules to be replaced and processor modules to be upgraded, while the computer system continues to operate, thus, greatly improving computer system reliability.

The combination of Hubis/Klein does not disclose a storage system comprising a first cluster system and a second cluster system,

wherein the switch unit of the first cluster system is coupled to the switch of the second cluster system by a communication path.

Matsunami discloses a storage system comprising a first cluster system and a second cluster system (paragraph 0043; paragraph 0070; Fig. 14, elements 10 and 20); *It should be noted that each "disk array switch" combined with its respective "disk array subset" comprises a "cluster".*

wherein the switch unit of the first cluster system is coupled to the switch of the second cluster system by a communication path (paragraph 0043; paragraph 0070; Fig. 3, elements 201 and 2040; Fig. 14, element 2040). *It should be noted that the "crossbar switch" is equivalent to the "switch unit" and the "Intercluster I/F" is equivalent to the "communication path".*

The combination of Hubis/Klein and Matsunami are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Matsunami's clustered storage system and Hubis/Klein's array controller and processor modules such that the storage system comprises a first cluster and a second cluster, each cluster comprising an array controller, a plurality of processor modules, and a plurality of disk drives, because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of providing a disk storage system that responds easily to needs for high reliability and future expansion.

The combination of Hubis/Klein/Matsunami does not disclose when a first processing load at said first interface adapters which are coupled to said at least one host computer is greater than a second processing load at said second interface adapters which are coupled to said at least one disk drive, the number of processors allocated to said first processing load at said first interface adapters is larger than the number of processors allocated to said second processing load at said second interface adapters,

and wherein when said second processing load of said second interface adapters is greater than said first processing load at said first interface adapters, the number of processors allocated to said second processing load of said second interface adapters is larger than the number of said first processing load of said first interface adapters.



Alford discloses when a first processing load at said first interface adapter is greater than a second processing load at second interface adapter, the number of processors allocated to said first processing load at said first interface adapter is larger than the number of processors allocated to said second processing load at said second interface adapter (paragraphs 0043-0044 and 0048-0049; Fig. 4; Fig. 7),

and when said second processing load of said second interface adapter is greater than said first processing load at said first interface adapter, the number of processors allocated to said second processing load of said second interface adapter is larger than the number of said first processing load of said first interface adapter (paragraphs 0043-0044 and 0048-0049; Fig. 4; Fig. 7).

The combination of Hubis/Klein and Alford are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Alford's dynamic re-assignment of resources within Hubis/Klein's storage system, such that one partition is coupled to the host computer and another partition is coupled to the disk drive. The motivation for doing so would have been to communicate information about peaks in resource demands from an operating system running in a partition to the partitioning management software such that the software can re-assign additional resources to the partition as needed.

24. **As per claim 54**, the combination of Hubis/Klein/Matsunami/Alford discloses said processor units in said first cluster system can instruct said plurality of first interface

units and the plurality of second interface units of said second cluster system to transfer a data (Matsunami, paragraph 0070).

### **Response to Arguments**

25. Applicant's arguments filed August 4, 2009 with respect to **claims 21, 23-25, 27, 29-39, and 44-55** have been considered but are moot in view of the new grounds of rejection above.

### **Conclusion**

#### **STATUS OF CLAIMS IN THE APPLICATION**

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

#### **CLAIMS REJECTED IN THE APPLICATION**

Per the instant office action, **claims 21, 23-25, 27, 29-39, and 44-55** have received an action on the merits and are subject of a non-final action.

#### **RELEVANT ART CITED BY THE EXAMINER**

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

U.S. Patent Application Publication 2003/0061264 (Benhase et al.) discloses allocating processor resources to a first and second types of tasks. An allocation of processor resources to the first and second types of tasks is indicated. Data is gathered indicating a first workload level for the first type of tasks and a second workload level for the second type of tasks. A determination is made of a change to the indicated allocation of processor resources to the first and second types of tasks based on at least one of the first workload level and second workload level data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arpan Savla/  
Examiner, Art Unit 2185  
October 21, 2009

/Sanjiv Shah/  
Supervisory Patent Examiner, Art  
Unit 2185